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Guide to Standards and Publications Relating to Quality and Reliability of Electronic Hardware

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GUIDE TO STANDARDS AND PUBLICATIONS RELATING TO QUALITY AND RELIABILITY OF ELECTRONIC HARDWARE

Contents

Foreword

This document gathers and organizes common standards and publications relating to quality processes and methods relating to the solid-state, microelectronics, and associated industries. This is intended to facilitate access to the applicable documents when working with electronic hardware. This will have a positive effect on quality and reliability as users gain more access to proper methods in designing, producing, and testing parts.

The quality and reliability documents in this publication have been categorized into nine subsections. Each category is organized in a table format in Section 3 and a brief description of each of these documents is contained in Appendix A. The last section is an alphabetized listing of the sources for the standards with their addresses, phone numbers, and URL web sites. This publication will be periodically reviewed and updated as required.

Introduction

Do to the wide breadth of the subject matter and numerous standards bodies in existence this publication cannot, and does not seek to, contain all possible relevant material. It is not intended to recommend or imply the applicability of any standard for a specific purpose.

GUIDE TO STANDARDS AND PUBLICATIONS RELATING TO QUALITY AND RELIABILITY OF ELECTRONIC HARDWARE

(From JEDEC Board Ballot JCB-13-43, formulated under the cognizance of the JC-14.4 Subcommittee on Quality Processes and Methods.)

1 Scope

This publication contains a listing and description of commonly used quality and reliability related publications applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose.

2 Normative reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. The document revisions have not been included in this listing. The latest document revision shall be used when referencing this document. The web sites listed above are referred to for the latest and official documents for all standards.

Reference	Name	Web Site
AEC	Automotive Electronics Council	aecouncil.com
ANSI	American National Standards Institute:	ansi.org
ASQ	American Society for Quality:	asq.org
CEA	Consumer Electronics Association	ce.org
CECC	CENELEC Electronic Components Committee	coduss.co.uk/cecc
ESDA	ESD Association	esda.org
IEC	International Electrotechnical Commission	iec.ch
IPC	Institute for Interconnecting and Packaging Electronic Circuits	ipc.org
ISO	International Organization for Standardization	iso.org
JEDEC	Solid State Technology Association	jedec.org
JEITA	Japan Electronics and Information Technology Association	jeita.or.jp
MIL	US Military	
NIST	National Institute of Standards and Technology	nist.gov
SAE	SAE International	sae.org
TECHAMERICA		techamerica.org
UL	Underwriters Laboratories	ul.com

3 Listing of Quality and Reliability Standards and Publications

This list is the number and title of standards and publication relating to the manufacture and testing of hardware components. They are grouped by category and sorted alphabetically. There is a description of each one found in Annex A.

3.1 Electrical Tests – Methods

Number	Title
JEDEC EIA318	Measurement of Reverse Recovery Time for Semiconductor System Diodes
JEDEC EIA397	Recommended Standard for Thyristors
JEDEC EIA397-1	Addendum No. 1 to EIA-397
JEP121	Requirement for Microelectronic Scanning and Test Optimization
JEP128	Guide for Standard Probe Pad Sizes and Layouts for Wafer-Level Electrical Testing
JEP154	Guideline For Characterizing Solder Bump Electromigration Under Constant Current And Temperature Stress
JESD30	Measurement of Small-Signal HF, VHF, and UHF Power Gain of Transistors
JESD78	IC Latch-Up Test
JESD86	Electrical Parameters Assessment
JESD89	Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-1	Test Method For Real-Time Soft Error Rate
JESD89-2	Test Method For Alpha Source Accelerated Soft Error Rate
JESD89-3	Test Method For Beam Accelerated Soft Error Rate
JESD282	Silicon Rectifier Diodes
JESD284	Test Methods for the Collector - Base Time Constant and for the Resistive Part of the Common Emitter Input Impedance
JESD286	Standard for Measuring Forward Switching Characteristics of Semiconductor Diode
JESD307	Voltage Regulator Diode Noise Voltage Measurements:
JESD311	Measurement of Transistor Noise Figure at MF, HF and VHF
JESD313	Thermal Resistance Measurements of Conductive Cooled Power Transistor
JESD320	Thermal Equilibrium Conditions for Measurement of Diode Static Parameters
JESD353	The Measurement of Transistor Noise Figure at Frequencies up to 20 KHz by Sinusoidal Signal Generator Method
JESD354	Measurement of Transistor Equivalent Noise Voltage and Equivalent Noise Current at Frequencies of up to 20 KHz

3.1 Electrical Tests – Methods (cont'd)

JESD371	Measurement of Small-Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio
JESD372	Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters
JESD381	Method of Diode "Q" Measurements
JESD398	Measurement of Small Values of Transistor Capacitance
MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-750	Test Method Standard Test Methods for Semiconductor Devices
MIL-STD-883	Test Method Standard, Microcircuits

3.2 ESD Control – Measurement, Handling, Symbol and Label

Number	Title
AEC-Q100-002	Human Body Model (HBM) Electrostatic Discharge Test (IC)
AEC-Q100-004	IC Latch-Up Test (IC)
AEC-Q100-011	Charged Device Model (CDM) Electrostatic Discharge Test (IC)
AEC-Q101-001	Human Body Model (HBM) Electrostatic Discharge Test (Discreet)
AEC-Q101-005	Charged Device Model (CDM) Electrostatic Discharge Test (Discreet)
AEC-Q200-002	Human Body Model (HBM) Electrostatic Discharge Test (Discreet)
ESD ADV1.0	Glossary for Electrostatic Discharge Terminology
ESD S1.1	Wrist Straps
ESD STM3.1	Ionization
ESD S4.1	Work Surfaces - Resistive
ESD S5.3.1	Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Component Level
ESD S6.1	Grounding - Recommended Practice
ESD S7.1	Resistive Characterization of Materials -Floor Materials
ESD S8.1	Symbols–ESD Awareness
ESD S20.20	Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
ESD S541	Packaging Materials for ESD Sensitive Items
ESD STM11.11	Surface Resistance Measurement of Static Dissipative Planar Materials
JEP113	Symbols and Labels for Moisture Sensitive Devices
JEP130	Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing
JESD22-A114	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

3.2 ESD Control – Measurement, Handling, Symbol and Label (cont'd)

JESD22-C101	Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components
JESD30	Descriptive Designation System for Semiconductor-Device Packages
JESD471	Symbol and Label for Electrostatic Sensitive Devices
JESD625	Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices
JS-001	Electrostatic Discharge Sensitivity Test - Human Body Model (Hbm) - Component Level

3.3 Mark-Pack-Ship – Container Labeling/Bar Coding, Tape and Reel, Dry-Packing

Number	Title
CEA-556	Outer Shipping Container Bar Code Label Standard
ECA EIA-296	Lead Taping of Components in Axial Lead Configuration for Automatic Handling
ECA EIA-468	Lead Taping Of Components In The Radial Configuration For Automatic Handling
ECA EIA-481	8 Mm Through 200 Mm Embossed Carrier Taping And 8 Mm & 12 Mm Punched Carrier Taping Of Surface Mount Components For Automatic Handling
EIA-476	Date Code Marking
EIA-763	Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling
JEITA ED-7303	Name and Code for Integrated Circuits Package
JEP160	Long-Term Storage Guidelines For Electronic Solid-State Wafers, Dice, And Devices
JESD22-B114	Mark Legibility
J-STD-033	Joint Ipc/Jedec Standard For Handling, Packing, Shipping, And Use Of Moisture/Reflow Sensitive Surface-Mount Devices
MIL-DTL-19491	Packaging of Semiconductor Devices

3.4 Process Control – SPC, Cpk, Control Charting, Environmental Controls, Calibration

Number	Title
ASQC B1-B3	Guide for Quality Control Charts Control Chart Method of Analyzing Data Control Chart Method for Controlling Quality During Production
ASQ H1197	Glossary & Tables for Statistical Quality Control
ASQ- M1	Calibration System
IPC-9191	General Guidelines for Implementation of Statistical Process Control (SPC)
ISO 2859	Sampling Procedures for Inspection by Attributes - Part 1: Sampling Schemes Indexed by Acceptance Quality Limit (AQL) for Lot-by-Lot Inspection
ISO 3534-2	Statistics -- Vocabulary and symbols -- Part 2: Applied statistics
ISO 3951-1	Sampling procedures for inspection by variables Part 1: Specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection for a single quality characteristic and a single AQL
ISO 3951-2	Sampling procedures for inspection by variables Part 2: General specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection of independent quality characteristics
JEP132	Process Characterization Guideline
JESD46	Customer Notification Of Product/Process Changes By Semiconductor Suppliers
JESD48	Product Discontinuance
JESD50	Special Requirements For Maverick Product Elimination And Outlier Management
MIL-HDBK-1331	Handbook for Parameters to be Controlled for the Specification of Microcircuits
TECHAMERICA EIA-557	Statistical Process Control Systems
TECHAMERICA EIA-738	Guideline on the Use and Application of Cpk
TECHAMERICA RB9	Failure Mode and Effect Analyses

3.5 Qualification and Reliability Monitoring – Initial Product/Process Qualification, Ongoing Reliability Monitoring, Qualification of Product/Process Changes

Number	Title
AEC-Q100 base	Stress Qualification For Integrated Circuits (base document only with no test methods)
AEC-Q101 base	Stress Test Qualification For Discrete Semiconductors (complete document with test methods)
AEC-Q200	Stress Test Qualification For Passive Components (complete document with test methods)
JEP143	Solid State Reliability Assessment Qualification Methodologies
JEP148	Reliability Qualification Of Semiconductor Devices Based On Physics Of Failure Risk And Opportunity Assessment
JEP158	3d Chip Stack With Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions
JESD22-A121	Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes
JESD22-B118	Semiconductor Wafer And Die Backside External Visual Inspection
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD49	Procurement Standard for Known Good Die (KGD)
JESD69	Information Requirements For The Qualification Of Silicon Devices
JESD72	Test Methods And Acceptance Procedures For The Evaluation Of Polymeric Materials
JESD659	Failure Mechanism Driven Reliability Monitoring of Silicon Devices
JS9702	Monotonic Bend Characterization of Board-Level Interconnects (IPC/JEDEC-9702)
JS9704	Printed Wiring Board (PWB) Strain Gage Test Guideline
MIL-HDBK-175	Microelectronic Devices
MIL-PRF-19500	General Specification for Semiconductor Devices
MIL-PRF-38534	General Specification for Hybrid Microcircuits
MIL-PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
SAE J1879	Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
TECHAMERICA SSB-1.001	Qualification and Reliability Monitors

3.6 Quality and Reliability Reporting -AOQ Measurement, Sampling Methods, Reliability Data (FITS), Failure Analysis, Product/Process Change Notification

Number	Title
ASQ- E2	Guide to Inspection Planning
ASQ Q3	Sampling Procedures and Tables for Inspection of Isolated Lots by Attributes
ASQ S1	An Attribute Skip-Lot Sampling Program
ASQ Z1.4	Sampling Procedures and Tables for Inspection by Attributes
ASQ Z1.9	Sampling Procedures and Tables for Inspection by Variables for Percent Nonconforming
ISO 3534-1	Statistics -- Vocabulary and symbols -- Part 1: General statistical terms and terms used in probability
JEP122	Failure Mechanisms and Model for Silicon Semiconductor Devices
JEP131	Process Failure Mode and Effects Analysis (FMEA)
JEP134	Guidelines for Preparing Customer-Supplied Background Information Relating to a Semiconductor Device Failure Analysis
JESD38	Standard For Failure Analysis Report Format
JESD46	Customer Notification of Product/Process Changes by Semiconductor Suppliers
JESD48	Product Discontinuance
JESD85	Methods For Calculating Failure Rates In Units Of Fits
MIL-PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
TECHAMERICA EIA-554	Method Selection for Assessment of Nonconforming Levels in Part Per Million (PPM)
TECHAMERICA EIA-555	Lot Acceptance Procedure for Verifying Compliance with the Specified Quality Levels (SQL) in PPM
TECHAMERICA EIA-584	Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of a Continuous Manufacturing Process
TECHAMERICA EIA-585	Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of Isolated Lots
TECHAMERICA SSB-1.004	Failure Rate Estimating

3.7 Quality Systems -General Requirements, Auditing, Terminology, Certification, Supplier/Subcontractor Control

Number	Title
ASQ C1	Specifications of General Requirements for a Quality Program
ISO 9000	Quality management systems - Fundamentals and vocabulary
ISO 9001	Quality management systems - Requirements
ISO 9004	Managing for the sustained success of an organization -- A quality management approach
ISO 19011	Guidelines for quality and/or environmental management systems auditing
ISO14001	Environmental Management System:
ISO 1011	Guidelines for quality and/or environmental management systems auditing
JEP146	Guidelines For Supplier Performance Rating
JESD31	General Requirements for Distributors of Commercial and Military Semiconductor Devices
JESD99	Terms, Definitions, and Symbols for Microelectronics Devices
JESD100	Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits
JESD670	Quality System Assessment
JESD671	Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems)
MIL- PRF-19500	General Specification for Semiconductor Devices
MIL- PRF-38534	General Specification for Hybrid Microcircuits
MIL- PRF-38535	General Specification for Integrated Circuits (Microcircuits) Manufacturing
NIST Malcolm Baldrige	National Quality Award Criteria
TECHAMERICA EIA681	Assessment Guide for Process Certification

3.8 Reliability Testing – Methods

Number	Title
ECA 186	Passive Electronic Component Parts, Test Methods for; General Instructions and Index of Tests
IEC-60068	Basic Environmental Testing Procedures
EIAJ ED-4701	Environmental and Endurance Test Methods for Semiconductor Devices
IEC-60721	Classification of Environmental Conditions
JEP79	Life Test Methods for Photoconductive Cells
JEP110	Guidelines for the Measurement of Thermal Resistance of GaAs FETS
JEP119	Procedure for Executing SWEAT
JEP121	Requirement for Microelectronic Screening and Test Optimization
JEP122	Failure Mechanisms and Models for Silicon Semiconductor Devices
JEP150	Stress-Test-Driven Qualification Of And Failure Mechanisms Associated With Assembled Solid State Surface-Mount Components
JEP153	Characterization And Monitoring Of Thermal Stress Test Oven Temperatures
JESD22-A100	Cycled Temperature Humidity Bias Life Test
JESD22-A101	Steady State Temperature Humidity Bias Life Test
JESD22-A102	Accelerated Moisture Resistance - Unbiased Autoclave
JESD22-A103	High Temperature Storage Life
JESD22-A104	Temperature Cycling
JESD22-A105	Power and Temperature Cycling
JESD22-A106	Thermal Shock
JESD22-A107	Salt Atmosphere
JESD22-A108	Temperature, Bias, and Operating Life
JESD22-A109	Hermeticity
JESD22-A110	Highly Accelerated Temperature and Humidity Stress Test (HAST)
JESD22-A113	Preconditioning of Plastic Surface-Mount Devices prior to Reliability Testing
JESD28	A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress
JESD33	Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line
JESD35	Procedure for Wafer-Level Testing of Thin Dielectrics
JESD37	Standard Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method
JESD60	A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation at Maximum Gate Current Under DC Stress

3.8 Reliability Testing – Methods (cont'd)

JESD61	Isothermal Electromigration Test Procedure
JESD63	Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature
JESD74	Early Life Failure Rate Calculation Procedure For Semiconductor Components
J-STD-020	Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices
MIL-HDBK-814	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices FSC 59GP
MIL-STD-750	Test Methods for Semiconductor Devices FSC 5961
MIL-STD-790	Established Reliability and High Reliability Qualified products List (QPL) System for Electrical, Electronic, and Fiber Optic Part Specification
MIL-STD-883	Test Methods Standard Microcircuits
TECHAMERICA SSB-1.002	Environmental Tests and Associated Failure Mechanisms

3.9 Visual and Mechanical Testing – Methods

Number	Title
AE -Q100-001	Wire Bond Shear Test
AEC-Q100-005	Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test
AEC-Q100-006	Electro-Thermally Induced Parasitic Gate Leakage Test (GL)
AEC-Q100-007	Fault Simulation and Test Grading
AEC-Q100-008	Early Life Failure Rate (ELFR)
AEC-Q100-009	Electrical Distribution Assessment
AEC-Q100-010	Solder Ball Shear Test
AEC-Q100-012	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
AEC-Q101-003	Wire Bond Shear Test
AEC-Q101-004	Miscellaneous Test Methods
AEC-Q101-006	Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems
AEC - Q200-001	Flame Retardance Test
AEC - Q200-003	Beam Load (Break Strength) Test
AEC - Q200-004	Measurement Procedures for Resettable Fuses
AEC - Q200-005	Board Flex / Terminal Bond Strength Test

3.9 Visual and Mechanical Testing – Methods (cont'd)

AEC - Q200-006	Terminal Strength (SMD) / Shear Stress Test
AEC - Q200-007	Voltage Surge Test
IEC 60695-1-11	Fire Hazard Testing
IPC J-STD-004	Requirements for Soldering Fluxes
IPC J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
JEITA ED-4702	Mechanical Stress Test Methods for Semiconductor Surface Mounting Devices
JEP84	Recommended Practice for Measurement of Transistor Lead Temperature
JEP110	Guidelines for the Measurement of Thermal Resistance of GaAs FETS
JEP114	Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification
JEP121	Requirement for Microelectronic Screening and Test Optimization
JEP156	Chip-Package Interaction Understanding, Identification And Evaluation
JESD9	Metal Package Specification for Microelectronic Packages and Covers
JESD22-B100	Physical Dimensions
JESD22-B101	External Visual
JESD22-B102	Solderability
JESD22-B103	Vibration, Variable Frequency
JESD22-B104	Mechanical Shock
JESD22-B105	Lead Integrity
JESD22-B106	Resistance to Solder Shock for Through-Hole Mounted Devices
JESD22-B107	Marking Permanency
JESD22-B108	Coplanarity Test for Surface-Mount Semiconductor Devices
JESD22-B111	Board Level Drop Test Method of Components for Handheld Electronic Products
JESD22-B115	Solder Ball Pull
JESD22-B116	Wire Bond Shear Test
JESD22-B117	Solder Ball Shear
MIL-STD-750	Test Methods for Semiconductor Devices
MIL-STD-883	Test Methods and Procedures Microcircuits
UL 94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
UL1694	UL Standard for Safety Tests for Flammability of Small Polymeric Component Materials

3.10 PB Component Application – Assembly, Soldering, Board Level Testing

Number	Title
IPC A-600	Acceptability of Printed Boards
IPC A-610	Acceptability of Electronic Assemblies
JEP154	Guideline For Characterizing Solder Bump Electromigration Under Constant Current And Temperature Stress
JESD201	Environmental Acceptance Requirements For Tin Whisker Susceptibility Of Tin And Tin Alloy Surface Finished
JESD22-A121	Measuring Whisker Growth On Tin And Tin Alloy Surface Finishes
JP002	Current Tin Whiskers Theory And Mitigation Practices Guideline
J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
J-STD-002	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
J-STD-005	Requirements for Soldering Pastes
J-STD-075	Classification of Non-IC Electronic Components for Assembly Processes
TECHAMERICA GEIA-GEB-0002	Reducing the Risk of Tin Whisker-Induced Failures in Electronic Equipment
TECHAMERICA GEIA-HB-0005-1	Program Management/Systems Engineering Guidelines For Managing The Transition To Lead-Free Electronics
TECHAMERICA GEIA-HB-0005-2	Reducing the Risk of Tin Whisker-Induced Failures in Electronic Equipment
TECHAMERICA GEIA-HB-0005-3	Rework/Repair Handbook to Address the Implications of Lead-Free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems
TECHAMERICA GEIA-STD-0005-1	Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder
TECHAMERICA GEIA-STD-0005-2	Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems
TECHAMERICA GEIA-STD-0005-3	Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes
TECHAMERICA GEIA-STD-0006	Requirements for Using Solder Dip to Replace the Finish on Electronic Piece Parts

Annex A (informative) Standards

The standards referenced in this document are in alpha-numeric order with a brief description. They are grouped by the currently maintaining body and do not include revision numbers. Documents beginning with JEP, J-STD, JESD, JS, JEDEC-EIA are JEDEC or joint JEDEC documents.

AEC - Q100

Stress Qualification For Integrated Circuits:
This document contains a set of failure mechanism based stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of integrated circuits (ICs). These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to precipitate failures in an accelerated manner compared to use conditions.

AEC - Q100-001

Wire Bond Shear Test:
This test establishes a procedure for determining the strength of the interface between a gold ball bond and a package bonding surface, or an aluminum wedge/stitch bond and a package bonding surface, on either pre-encapsulation or post-encapsulation devices. This strength measurement is extremely important in determining two features:
1) the integrity of the metallurgical bond which has been formed.
2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces.

AEC - Q100-002

Human Body Model (HBM) Electrostatic Discharge Test:
The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for electronic devices.

AEC - Q100-004

IC Latch-Up Test:
The purpose of this specification is to establish a reliable and repeatable procedure for performing an IC Latch-Up Test.

AEC - Q100-005

Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test:
This test is intended to evaluate the ability of the memory array of a standalone Non-volatile Memory (NVM) integrated circuit or an integrated circuit with a Non-volatile Memory module (such as a microprocessor Flash Memory) to: sustain repeated data changes without failure (Program/Erase Endurance), retain data for the expected life of the Non-volatile Memory (Data Retention), and withstand constant temperature with an electrical bias applied (Operating Life).

AEC - Q100-006

Electro-Thermally Induced Parasitic Gate Leakage Test (GL):
The purpose of this specification is to establish a reliable and repeatable procedure for determining surface mount integrated circuit susceptibility to Electro-Thermally Induced Parasitic Gate Leakage (GL). This specification may also be used as an evaluation tool for determining the susceptibility of circuit designs, molding compounds, fabrication processes, and post mold cure processes to GL.

Annex A (informative) Standards (cont'd)

AEC - Q100-007

Fault Simulation and Test Grading:

This test method defines fault grading procedure and specifies a level to which the manufacturing test program for the device under test must detect faults. Parametric failures are not covered. Another term for fault grading is fault simulation. Fault grading applies to all digital circuits including the digital portion of mixed signal and linear circuits. Fault grading does not apply to the linear portion of the circuits. Also, this document covers modeling and logic simulation requirements; the assumed fault model and fault simulation requirements; and the procedure that must be followed to evaluate and report test coverage.

AEC - Q100-008

Early Life Failure Rate (ELFR):

This test method is applicable to all IC part qualifications. In the case of many parts, generic data (see Q100, section 2.3) may fulfill the requirements of this test method. If the supplier is qualifying a part for which no generic data is available (unproven technology or design rules) for general usage then the requirements of this test method should be utilized to meet the requirements of Q100.

AEC - Q100-009

Electrical Distribution Assessment:

This specification describes test methods for assessing electrical parameter characterization, distributions (e.g., to AC, DC and timing, etc.) and parametric shifts of integrated circuits which have established supplier datasheet limits. For new parts, these datasheet limits are determined through application of the Characterization procedure AEC-Q003 as referenced in the AEC-Q100. The results are used to determine the capability to meet the performance requirements of the device specification. The results can also be used to set device test limits (e.g., LTL and UTL).

AEC - Q100-010

Solder Ball Shear Test:

The purpose of this test method is to define the procedure for measuring the shear strength of the interface between the barrier metal and solder ball. This method also establishes the minimum shear strength requirements for this interface.

AEC - Q100-011

Charged Device Model (CDM) Electrostatic Discharge Test:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic devices. This test method does not include socketed CDM.

AEC - Q100-012

Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems:

The purpose of this specification is to determine the reliability of "protected" drivers when operating in a continuous short circuit condition. This document is not intended to address soft short circuit failures seen in incandescent lamp applications (e.g., external lighting). These applications will be considered in a separate document.

Annex A (informative) Standards (cont'd)

AEC - Q101

Stress Test Qualification For Discrete Semiconductors:

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

AEC - Q101-001

Human Body Model (HBM) Electrostatic Discharge Test:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for discrete components.

AEC - Q101-003

Wire Bond Shear Test:

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stich bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features:
1) The integrity of the metallurgical bond which has been formed.
2) The reliability of gold and aluminum wire bonds to die or package bonding surfaces.

AEC - Q101-004

Miscellaneous Test Methods:

This document establishes the procedure and criteria for performing miscellaneous qualification tests referred to in Table 2 (Process Change Guidelines for the Selection of Tests) of AEC-Q101. The tests described in this document are:
Section 2 - Unclamped Inductive Switching (UIS)
Section 3 - Dielectric Integrity (DI)
Section 4 - Destructive Physical Analysis (DPA)

AEC - Q101-005

Charged Device Model (CDM) Electrostatic Discharge Test:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic components.

AEC - Q101-006

Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems:

The purpose of this specification is to determine the reliability of "protected" drivers when operating in a continuous short circuit condition.

AEC - Q200

Stress Test Qualification For Passive Components:

This specification defines the minimum stress test driven qualification requirements and references test conditions for qualification of passive electrical devices.

Annex A (informative) Standards (cont'd)

AEC - Q200-001

Flame Retardance Test:

The purpose of this specification is to assure a device will not flame due to self-heating when full automotive battery potential is applied. This test applies to all devices which, under normal operation, are not intended to be used at full automotive battery potential.

AEC - Q200-002

Human Body Model (HBM) Electrostatic Discharge Test:

The purpose of this specification is to establish a reliable and repeatable procedure for determining PASSIVE COMPONENT HBM ESD sensitivity.

AEC - Q200-003

Beam Load (Break Strength) Test:

This specification establishes the procedure and criteria for evaluating break strength.

AEC - Q200-004

Measurement Procedures for Resettable Fuses:

This method covers the test and measurement methods for resettable fuses based on polymeric materials with positive temperature coefficient of resistance. The purpose of this specification is to provide users of such components means to compare polymeric positive temperature coefficient (PPTC) based resettable fuses against an established standard performance requirements tested in accordance with an established test method.

AEC - Q200-005

Board Flex / Terminal Bond Strength Test:

This specification establishes the procedure and criteria to determine the ability of surface mounted device terminations and seals to withstand bending, flexing and pulling forces which occur on printed circuit boards during handling and assembly.

AEC - Q200-006

Terminal Strength (SMD) / Shear Stress Test:

The purpose of this test is to verify that the component terminations can withstand axial stresses that are likely to be applied during normal manufacturing and handling of a finished printed circuit board (PCB) assembly.

AEC - Q200-007

Voltage Surge Test:

The purpose of this specification is to assure a device will withstand voltage surges at the surge voltage rating of the device's specification.

ASQ B1-B3 (ANSI/ASQC B1-B3)

Quality Control Chart Methodologies:

This standard is intended as a guide for handling problems concerning the economic control of quality of materials, manufactured products, services, etc.

Annex A (informative) Standards (cont'd)

ASQ C1 (ANSI/ASQC C1)

Specifications of General Requirements for a Quality Program:

This standard concerns the establishment and maintenance of a quality program by a contractor to assure compliance with contract requirements in the areas of quality management, design information, procurement, manufacture, acceptance, and documentation.

ASQ E2 (ANSI/ASQC E2)

Guide to Inspection Planning:

This standard describes the significant elements that should be considered in the development of inspection activities. It provides generic guidelines for planning and applying a product/process inspection system for construction, manufacturing, operating, or service functions.

ASQ H1197

Glossary & Tables for Statistical Quality Control, Second Edition:

This expanded and updated second edition provides clear definitions based on national and international standards. Recommended definitions, symbols, and formulas for the basic statistical measures, significance tests, confidence limits, control charts, acceptance sampling, and design of experiments are all thoroughly covered. Selected statistical tables and a glossary of symbols included.

ASQ M1 (ANSI/ASQC- M1)

Calibration System:

This standard specifies general requirements for assuring the quality of calibration in accordance with established practices or objective quality control techniques

ASQ Q3 (ASQC Q3)

Sampling Procedures and Tables for Inspection of Isolated Lots by Attributes:

An acceptance sampling system to be used when one or more lots that are isolated or separated from a continuous stream of lots are submitted for acceptance. For this purpose the quality levels referenced in this standard are indexed by Limiting Quality (LQ). The LQ represents the quality of a lot the consumer does not wish to accept. The procedures of this standard differ from those of ANSI/ASQC Z1.4, which is appropriate for a continuous stream of lots with an AQL (Acceptable Quality Level) specified.

ASQ S1 (ANSI/ASQC S1)

An Attribute Skip-Lot Sampling Program:

This document provides a procedure for reducing the inspection effort on products submitted by those suppliers who have demonstrated their ability to control, in an effective manner, all facets of product quality and consistently produce superior quality material. This procedure shall not be applied to the inspection of product characteristics which involve the safety of personnel. The standard is to be used only with ANSI/ASQC Z1. 4

ASQ Z1.4 (ANSI/ASQC Z1.4)

Sampling Procedures and Tables for Inspection by Attributes:

This standard, which corresponds to MIL-STD-105D, establishes sampling plans and procedures for inspection by attributes. Its tables and procedures are completely compatible with MIL-STD-105D.

Annex A (informative) Standards (cont'd)

ASQ Z1.9 (ANSI/ASQC Z1.9)

Sampling Procedures and Tables for Inspection by Variables for Percent Nonconforming:
This standard, establishing sampling plans and procedures for inspection by variables, corresponds to the military standard MIL-STD-414 and is interchangeable with ISO/DIS 3951. It contains tables and procedures of MIL-STD-414, suitably modified to achieve correspondence with ISO/DIS 3951 and matching with MIL-STD-105D and ANSI/ASQC Z1.4.

CEA-556

Outer Shipping Container Bar Code Label Standard:
Packing or shipping containers may have multiple labels, such as: designation label, transaction label, product package label or product label. This standard addresses the transaction label, which provides information for receiving shipments. The shipping and receiving operations using bar code technology. The transaction label should be affixed to final shipping containers, boxes, cartons, pallets, cases, barrels, etc.

ECA186

Passive Electronic Component Parts, Test Methods for; General Instructions and Index of Tests
This Standard establishes uniform methods for testing electronic component parts. In case of conflict between this Standard and any individual component standards or detail specifications, the requirements of the individual component standard or detail specification shall govern.

ECA EIA-296

Lead Taping of Components in Axial Lead Configuration for Automatic Handling:
This Standard is formulated to provide dimensions and tolerances necessary to tape axial leaded components after manufacture so that they can be automatically handled. Axial leaded components are leaded components with the lead egress concentric with the longitudinal axis centerline of the component body.

ECA EIA-468

Lead Taping Of Components In The Radial Configuration For Automatic Handling:
This standard was formulated to provide dimensions and tolerances necessary to lead tape components in the radial format (unidirectional leads) such that they may be automatically handled. Automatic handling includes insertion, preforming and other operations. The emphasis of this standard is on the requirements for high-speed automatic insertion. This standard covers the lead taping requirements for components having two or more radial configured leads, provided these components may be taped in accordance with the requirements of this document.

ECA EIA-481

8 Mm Through 200 Mm Embossed Carrier Taping And 8 Mm & 12 Mm Punched Carrier Taping Of Surface Mount Components For Automatic Handling:
This Standard covers requirements for taping surface mount components. Complementary standards for specialized taping requirements are included in the addendum.

Annex A (informative) Standards (cont'd)

EIA-476

Date Code Marking:

This standard describes a system for identification of the date of manufacture of an electronic component or equipment through the manufacturer′s marking the product with a series of numbers known as the EIA date code. EIA additionally provides a scheme for standardization of the calendar year and week in a date code. If the date code is desired by the customer it must specified in the contractual agreements (purchase order or ordering specification).

EIA-763

Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling:

This standard covers requirements for punched and embossed carrier taping of components such as silicon dies, bumped flip chip devices, and chip scale packages.

EIAJ ED-4701

Environmental and Endurance Test Methods for Semiconductor Devices:

These standards provide for environmental test methods and endurance test methods aimed at evaluating the resitance and the endurance of discrete semiconductor devices and integrated circuits used in electronic equipment mainly for general industrial applications and consumer applications, under the various environmental conditions of various kinds that occur during their use, storage and transportation.

ESD ADV1.0

Glossary for Electrostatic Discharge Terminology:

The purpose of this Glossary is to promote technically correct terminology in the electrical Overstress/Electrostatic Discharge (EOS/ESD) community.

ESD S1.1 (ANSI / ESD S1.1)

Wrist Straps:

This standard establishes requirements for personnel grounding wrist straps. It covers mechanical and electrical requirements and provides specifications for qualification and periodic monitoring of wrist straps.

ESD S4.1 (ANSI / ESD S4.1)

Work Surfaces - Resistive Measurements:

This standard establishes test methods for measuring the electrical resistance of work surface materials used at workstations for protection of ESD susceptible items. The standard includes methods for evaluating and selecting materials, testing of new work surface installations, and testing of previously installed work surfaces.

ESD S5.3.1 (ANSI / ESD S5.3.1)

Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Component Level:

This standard test method established the procedures for testing, evaluating, and classifying the ESD sensitivity components to a defined charge device model.

Annex A (informative) Standards (cont'd)

ESD S6.1 (ANSI / ESD S6.1)

Grounding - Recommended Practice:

This document recommends the parameters, procedures, and types of materials needed to establish an ESD grounding system for the protection of electronic hardware from ESD damage in the commercial environment. This grounding system is used for personnel grounding devices, work surfaces, chairs, carts, floors, and other related equipment.

ESD S7.1 (ANSI/ESD S7.1)

Resistive Characterization of Materials -Floor Materials:

Measurement of the electrical resistance of various floor materials, such as floor coverings, mats, and floor finishes. It provides test methods for qualifying floor materials before installation or application and for evaluating and monitoring materials after installation or application.

ESD S8.1 (ANSI/ESD S8.1)

Symbols–ESD Awareness:

Three types of ESD awareness symbols are established by this document. The first one is to be used on a device or assembly to indicate that it is susceptible to electrostatic charge. The second is to be used on items and materials intended to provide electrostatic protection. The third symbol indicates the common point ground.

ESD S20.20 (ANSI/ESD S20.20)

Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices):

This standard provides administrative and technical requirements for establishing, implementing, and maintaining an ESD Control Program to protect electrical or electronic parts, assemblies, and equipment susceptible to ESD damage from Human Body Model (HBM) discharges greater than or equal to 100 volts.

ESD S541 (ANSI/ESD S541)

Packaging Materials for ESD Sensitive Items:

This standard describes the packaging material properties needed to protect electrostatic discharge (ESD) sensitive electronic items, and references the testing methods for evaluating packaging and packaging materials for those properties. Where possible, performance limits are provided. Guidance for selecting the types of packaging with protective properties appropriate for specific applications is provided. Other considerations for protective packaging are also provided.

ESD STM 3.1 (ANSI / ESD STM3.1)

Ionization:

Test methods and procedures for evaluating and selecting air ionization equipment and systems are covered in this standard test method. The document establishes measurement techniques to determine ion balance and charge neutralization time for ionizers.

ESD STM11.11 (ANSI/ESD STM11.11)

Surface Resistance Measurement of Static Dissipative Planar Materials:

This standard test method defines a direct current test method for measuring electrical resistance, replacing ASTM D257-78. The standard is designed specifically for static dissipative planar materials used in packaging of ESD sensitive devices and components.

Annex A (informative) Standards (cont'd)

IEC-60068

Basic Environmental Testing Procedures:
This standard contains a series of basic environmental testing procedures.

IEC-60721

Classification of Environmental Conditions:
This standard contains a listing of environmental conditions appearing in nature and classifications of groups of environmental parameters and their severity.

IEC 60695-1-11

Fire Hazard Testing:
This document provides guidance for assessing the fire hazard of electrotechnical products and for the resulting development of fire hazard testing as related directly to harm to people, animals or property. It outlines a hazard-based process to identify appropriate fire test methods and performance criteria for products.

IPC-9191

General Guidelines for Implementation of Statistical Process Control (SPC):
IPC-9191 reflects the principals of statistical process control (SPC) represented by ISO/DIS 11462-1, Guidelines for Implementation of Statistical Process Control (SPC) -- Part 1: Elements of SPC. This document outlines the SPC philosophy, implementation strategies, tools, and techniques used for relating process control and capability to final product requirements.

IPC A-600

Acceptability of Printed Boards:
This document describes the preferred, acceptable, and nonconforming conditions that are either externally or internally observable on printed boards. It represents the visual interpretation of minimum requirements set forth in various printed board specifications, e.g.; IPC-6010 series, J-STD-003, etc.

IPC A-610

Acceptability of Electronic Assemblies:
This document presents acceptance requirements for the manufacture of electrical and electronic assemblies. Historically, electronic assembly standards contained a more comprehensive tutorial addressing principles and techniques. For a more complete understanding of this document's recommendations and requirements, one may use this document in conjunction with IPC-HDBK-001, IPC-AJ-820, and IPC J-STD-001.

IPC J-STD-004

Requirements for Soldering Fluxes:
This standard covers requirements for qualification and classification of rosin, resin, organic and inorganic fluxes according to the activity level and halide content of the fluxes. It includes solder fluxes, flux-containing materials and low residue fluxes for no-clean processes.

Annex A (informative) Standards (cont'd)

IPC J-STD-006

Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications:

This standard prescribes the nomenclature, requirements and test methods for electronic grade solder alloys; for fluxed and non-fluxed bar, ribbon, and powder solders, for electronic soldering applications; and for "special" electronic grade solders. This is a quality control standard and is not intended to relate directly to the material's performance in the manufacturing process.

ISO 1011

Guidelines for quality and/or environmental management systems auditing:

Guidelines for quality and/or environmental management systems auditing, replaces six older standards in the ISO 9000 (quality) and ISO 14000 (environment) families. Its use will give organizations a more integrated and balanced view of their operations, making it an outstanding tool for continuous improvement towards business excellence. It is also aimed to help user organizations optimize their management systems, facilitate the integration of quality and environmental management, and, in allowing single audits of both systems, save money and decrease disruption of work units being audited.

ISO 2859

Sampling Procedures for Inspection by Attributes - Part 1: Sampling Schemes Indexed by Acceptance Quality Limit (AQL) for Lot-by-Lot Inspection:

This part of ISO 2859 specifies an acceptance sampling system for inspection by attributes. It is indexed in terms of the acceptance quality limit (AQL).

Its purpose is to induce a supplier through the economic and psychological pressure of lot non-acceptance to maintain a process average at least as good as the specified acceptance quality limit, while at the same time providing an upper limit for the risk to the consumer of accepting the occasional poor lot.

ISO 3534-1 (ANSI/ISO/ASQC A3534-1)

Statistics -- Vocabulary and symbols -- Part 1: General statistical terms and terms used in probability:

A standardization of the symbols, concepts, terms, and procedures relating to Shewhart control charts, control charts with warning limits, moving averages and ranges, exponentially smoothed averages, Cusum charts, multivariate control, trend control, process capability factor, and the acceptance control chart.

ISO 3534-2 (ANSI/ISO/ASQ A3534-2)

Statistics -- Vocabulary and symbols -- Part 2: Applied statistics:

This part of ISO 3534 defines applied statistics terms, and expresses them in a conceptual framework in accordance with ISO normative terminology practice. Term entries are arranged thematically. An alphabetical index is provided. Standardized symbols and abbreviations are defined.

Annex A (informative) Standards (cont'd)

ISO 3951-1

Sampling procedures for inspection by variables Part 1: Specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection for a single quality characteristic and a single AQL

This part of ISO 3951 specifies an acceptance sampling system of single sampling plans for inspection by variables, in which the acceptability of a lot is implicitly determined from an estimate of the percentage of nonconforming items in the process, based on a random sample of items from the lot.

ISO 3951-2

Sampling procedures for inspection by variables Part 2: General specification for single sampling plans indexed by acceptance quality limit (AQL) for lot-by-lot inspection of independent quality characteristics:

This part of ISO 3951 specifies an acceptance sampling system of single sampling plans for inspection by variables, indexed in terms of the Acceptance Quality Limit (AQL).

ISO 9000 (ANSI/ISO/ASQ Q9000)

Quality management systems - Fundamentals and vocabulary

Describes the fundamentals of a QMS and specifies the terminology for a QMS. This standard is intended for use in improvement of communication and understanding in the quality field. It has direct application with regard to the ISO9000 series of quality standards.

ISO 9001 (ANSI/ISO/ASQ Q9001)

Quality Management Systems - Requirements

This standard specifies requirements for a quality management system where an organization:
1 Needs to demonstrate its ability to consistently provide product that meets customer and applicable statutory and regulatory requirements, and
2 Aims to enhance customer satisfaction through the effective application of the system, including processes for continual improvement of the system and the assurance of conformity to customer and applicable statutory and regulatory requirements.

ISO 9004

Managing for the sustained success of an organization -- A quality management approach:

This International Standard provides guidance to organizations to support the achievement of sustained success by a quality management approach. It is applicable to any organization, regardless of size, type and activity.

ISO 14001

Environmental Management System:

This International Standard specifies requirements for an environmental management system, to enable an organization to implement a policy and objectives which take into account legal requirements and other requirements to which the organization subscribes, and information about significant environmental aspects. It applies to those environmental aspects that the organization identifies as those which it can control and those which it can influence. It does not itself state specific environmental performance criteria.

Annex A (informative) Standards (cont'd)

ISO 19011

Guidelines for quality and/or environmental management systems auditing:
Provides guidance on the principles of auditing, managing audit programmes, conducting quality management system audits and environmental management system audits, as well as guidance on the competence of quality and environmental management system auditors.

JEDEC EIA318

Measurement of Reverse Recovery Time for Semiconductor System Diodes:
This standard defines a test method for the measurement of reverse recovery time for semiconductor system diodes. This standard is also intended to establish a method which to characterize the test fixture used for this measurement.

JEDEC EIA397

Recommended Standard for Thyristors:
One section of this standard presents a thorough explanation of thyristor principals, defining the different classes of these devices, their physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols.

JEDEC EIA397-1

Addendum No. 1 to EIA-397:
A compilation of 12 new or revised thyristor test methods that have been adopted since the original standard was issued in 1972.

JEITA ED-4702

Mechanical Stress Test Methods for Semiconductor Surface Mounting Devices:
This standard prescribes the evaluation method of durability against the mechanical stresses or thermal stresses, received during or after the mount process of surface mounting devices used mainly for industrial and consumer use equipment.

JEITA ED-7303

Name and Code for Integrated Circuits Package:
This standard specifies names and codes for semiconductor packages used for integrated circuit which are specified in the JEITA ED-7300.

JEP79

Life Test Methods for Photoconductive Cells:
This publication is for photoconductive cells sensitive primarily in the visible and near-infrared region.

JEP84

Recommended Practice for Measurement of Transistor Lead Temperature:
This publication covers recommended methods for the measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications.

Annex A (informative) Standards (cont'd)

JEP110

Guidelines for the Measurement of Thermal Resistance of GaAs FETS:

This publication is in reference to power GaAs FET applications requiring high reliability and an accurate measurement of thermal resistance in which it is extremely important to provide the user with knowledge of the FET's operating temperature so that more accurate life estimates can be made.

JEP113

Symbols and Labels for Moisture Sensitive Devices:

Certain Plastic Surface Mount Components (PSMCs) are subject to permanent damage due to moisture induced failures encountered during high temperature surface mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those PSMC devices that require special packing and precautions.

JEP114

Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification:

The main objective of this Publication is to disseminate and share the relevant information on PIND testing to all interested parties. The concepts and materials presented primarily deal with most of the cause factors that affect the "Measurement Variability" pertinent to "PIND" and how to control them.

JEP119

Procedure for Executing SWEAT:

This document describes an algorithm for executing of the Standard Wafer Level Electromigration Accelerated Test (SWEAT) on computer controlled instrumentation. The algorithm described represents one approach to the execution of SWEAT.

JEP121

Requirement for Microelectronic Screening and Test Optimization:

The purpose of this document provides the basis for the optimization of 100% screening/stress operations and sample inspection test activities. This document is designed to assist the manufacturer in optimizing the test flow while maintaining and/or improving assurance of providing high quality and reliable product in an efficient manner.

JEP122

Failure Mechanisms and Model for Silicon Semiconductor Devices:

This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

JEP128

Guide for Standard Probe Pad Sizes and Layouts for Wafer-Level Electrical Testing:

This publication is a guide that applies to double- and single-column arrays of metal probe pads, on a semiconductor wafer or chip, that are electrically connected to one or more test structures.

Annex A (informative) Standards (cont'd)

JEP130

Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing:
This document establishes the guidelines for unit container packing of integrated circuits and for the next level of container.

JEP131

Process Failure Mode and Effects Analysis (FMEA):
This publication was created in response to the need for a straightforward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

JEP132

Process Characterization Guideline:
This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool.

JEP134

Guidelines for Preparing Customer-Supplied Background Information Relating to a Semiconductor Device Failure Analysis:
The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format.

JEP143

Solid State Reliability Assessment Qualification Methodologies:
The purpose of this publication is to provide an overview of some of the most commonly used systems and test methods historically performed by manufacturers to assess and qualify the reliability of solid state products. The appropriate references to existing and proposed JEDEC (or EIA) standards and publications are cited. This document is also intended to provide an educational background and overview of some of the technical and economic factors associated with assessing and qualifying microcircuit reliability.

JEP146

Guidelines For Supplier Performance Rating:
The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers.

Annex A (informative) Standards (cont'd)

JEP148

Reliability Qualification Of Semiconductor Devices Based On Physics Of Failure Risk And Opportunity Assessment:

A concept is outlined, which proactively integrates qualification into the development process and provides a systematic procedure as support tool to development and gives early focus on required activities. It converts requirements for a product into measures of development and qualification in combination with a risk and opportunity assessment step and accompanies the development process as guiding and recording tool for advanced quality planning and confirmation. The collected data enlarge the knowledge database for DFR / BIR (design for reliability / building-in reliability) to be used for future projects. The procedure challenges and promotes teamwork of all involved disciplines.

JEP150

Stress-Test-Driven Qualification Of And Failure Mechanisms Associated With Assembled Solid State Surface-Mount Components:

This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array (BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB.

JEP153

Characterization And Monitoring Of Thermal Stress Test Oven Temperatures:

This document provides an industry standard method for characterization and monitoring thermal stress test oven temperatures. The procedures described in this document should be used to insure thermal stress test conditions are being achieved and maintained during various test procedures.

JEP154

Guideline For Characterizing Solder Bump Electromigration Under Constant Current And Temperature Stress:

This document describes a method to test the electromigration (EM) susceptibility of solder bumps, including other types of bumps, such as solder capped copper pillars, used in flip-chip packages. The method is valid for Sn/Pb eutectic, high Pb, and Pb-free solder bumps. The document discusses the advantages and concerns associated with EM testing, as well as options for data analysis.

JEP156

Chip-Package Interaction Understanding, Identification And Evaluation:

This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products.

Annex A (informative) Standards (cont'd)

JEP158

3d Chip Stack With Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions:

To increase device bandwidth, reduce power and shrink form factor, microelectronics manufacturers are implementing three dimensional (3D) chip stacking using through silicon vias (TSVs). Chip stacking with TSVs combines silicon and packaging technologies. As a result, these new structures have unique reliability requirements. This document is a guideline that describes how to evaluate the reliability of 3D TSV silicon assemblies.

JEP160

Long-Term Storage Guidelines For Electronic Solid-State Wafers, Dice, And Devices:

This publication examines the LTS requirements of wafers, dice, and packaged solid-state devices. The user should evaluate and choose the best practices to ensure their product will maintain as-received device integrity and minimize age- and storage-related degradation effects.

JESD9

Metal Package Specification for Microelectronic Packages and Covers:

This Standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronic packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating microelectronic circuits. This document details those minimum requirements necessary for the use of metal packages exclusively.

JESD22-A100

Cycled Temperature Humidity Bias Life Test:

The cycled temperature humidity bias life test is performed for the purpose of evaluating the reliability of non-hermetic solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it.

JESD22-A101

Steady State Temperature Humidity Bias Life Test:

The steady-state temperature humidity bias life test is performed for the purpose of evaluating the reliability of non-hermetic solid state devices in humid environments. It employs conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it.

JESD22-A102

Accelerated Moisture Resistance - Unbiased Autoclave:

This test is performed for the purpose of evaluating the moisture resistance of nonhermetic solid state devices. It employs severe conditions of pressure, humidity and temperature that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. This test is destructive; it may be used for qualification, lot acceptance and as a product monitor.

Annex A (informative) Standards (cont'd)

JESD22-A103

High Temperature Storage Life:

This standard establishes the requirements for testing solid state devices to determine their susceptibility to unbiased storage at high temperature. The purpose of this revision is to: Change the test length and its tolerance; make interim read points optional rather than mandatory; eliminate the prohibition on reheating the devices prior to completion of electrical testing; and add an option to change time and temperature conditions.

JESD22-A104

Temperature Cycling:

This test is conducted to determine the resistance of a part to extremes of high and low temperatures, and to alternate exposures to these extremes.

JESD22-A105

Power and Temperature Cycling:

This test is performed to determine the ability of a solid state device to withstand alternate exposures at high and low-temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst-case conditions encountered in typical applications. This test method is considered destructive and is only intended for device qualification.

JESD22-A106

Thermal Shock:

This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

JESD22-A107

Salt Atmosphere:

The salt atmosphere test is conducted to determine the resistance of solid state devices to corrosion. It is an accelerated test that simulates the effects of severe seacoast atmosphere on all exposed surfaces. The salt atmosphere test is considered destructive. It is intended for lot acceptance, process monitor, and qualification testing.

JESD22-A108

Temperature, Bias, and Operating Life:

This test is performed to determine the effects of bias conditions and temperature on solid state devices over a period of time. It is intended primarily for device qualification and reliability monitoring.

JESD22-A109

Hermeticity:

The purpose of this test method is to determine the effectiveness of the seal of hermetically sealed solid state devices. The seal tests are considered nondestructive. They are intended to be used for 100% screen, lot acceptance, product monitoring or for qualification testing as applicable. The seal tests may also be employed as end points for other environmental durability tests. It was also developed to maintain continuity with other recognized industry standards. (Method 1014 of MIL-STD-883)

Annex A (informative) Standards (cont'd)

JESD22-A110

Highly Accelerated Temperature and Humidity Stress Test (HAST):

The purpose of the test method is to evaluate the reliability of nonhermetic solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it.

JESD22-A113

Preconditioning of Plastic Surface-Mount Devices prior to Reliability Testing:

This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

JESD22-A114

Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM):

This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

JESD22-A121

Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes:

The predominant terminal finishes on electronic components have been Sn-Pb alloys. As the industry moves toward Pb-free components and assembly processes, the predominant terminal finish materials will be pure Sn and alloys of Sn, including Sn-Bi and Sn-Ag. Pure Sn and Sn-based alloy electrodeposits and solder-dipped finishes may grow tin whiskers, which could electrically short across component terminals or break off the component and degrade the performance of electrical or mechanical parts.

JESD22-B100

Physical Dimensions:

The purpose of this test is to determine whether the external physical dimensions of the device, in all package configurations, are in accordance with the applicable procurement document.

JESD22-B101

External Visual:

The purpose of the examination is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External Visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance, or both.

Annex A (informative) Standards (cont'd)

JESD22-B102

Solderability:

The purpose of this test method is to provide a means of determining the solderability of device terminations that are intended to be joined to another surface using solder for the attachment. It also provides optional conditions for aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for normal and surface mount devices.

JESD22-B103

Vibration, Variable Frequency:

This standard is established to determine the effect of vibration, within the specified frequency range, on the internal structural elements. This is a destructive test, intended for device qualification. It is normally applicable to cavity-type packages.

JESD22-B104

Mechanical Shock:

This standard allows determination of the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks during handling, shipping, or field operation.

JESD22-B105

Lead Integrity:

This standard provides various tests for determining the integrity of solid state device leads, welds and seals. It is recommended that this test be followed by hermeticity test in accordance with Test Method A109 to determine any effect of the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, are considered destructive and are recommended only for qualification testing.

JESD22-B106

Resistance to Solder Shock for Through-Hole Mounted Devices:

This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. The heat can be either conducted through the leads into the device or radiated from the solder bath to the body of the device, or both. In order to establish a standard test procedure for the most reproducible methods, the solder dip method is used because of its more controllable conditions. This test is destructive and may be used for qualification, lot acceptance and as a product monitor.

JESD22-B107

Marking Permanency:

This test method provides two tests for determining the marking permanency of ink marked integrated circuits. A new non-destructive tape test method is introduced to quickly determine marking integrity.

Annex A (informative) Standards (cont'd)

JESD22-B108

Coplanarity Test for Surface-Mount Semiconductor Devices:

The purpose of this test is to measure the deviation of the leads from coplanarity for surface-mount semiconductor devices. The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity at room temperature for surface-mount semiconductor devices.

JESD22-B111

Board Level Drop Test Method of Components for Handheld Electronic Products:

This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

JESD22-B114

Mark Legibility:

This standard describes a nondestructive test to assess solid state device mark legibility. The specification applies only to solid state devices that contain markings, regardless of the marking method. It does not define what devices must be marked or the method in which the device is marked, i.e., ink, laser, etc. The standard is limited in scope to the legibility requirements of solid state devices, and does not replace related reference documents listed in this standard

JESD22-B115

Solder Ball Pull:

This document describes a test method only; acceptance criteria and qualification requirements are not defined. This test method applies to solder ball pull force testing prior to end-use attachment. Solder balls are pulled individually using mechanical jaws; force and failure mode data are collected and analyzed. Other specialized solder ball pull methods using a heated thermode, gang pulling of multiple solder joints, etc., are outside the scope of this document. Both low and high speed testing are covered by this document.

JESD22-B116

Wire Bond Shear Test:

This test provides a means for determining the strength of the bond between a gold ball bond on a die bonding surface or an aluminum wedge or stitch bond on a package bonding surface, and may be performed on pre-encapsulation or post-encapsulation parts.

JESD22-B117

Solder Ball Shear:

The purpose of this test is conducted to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment and end-use conditions. Solder ball shear is a destructive test.

Annex A (informative) Standards (cont'd)

JESD22-B118

Semiconductor Wafer And Die Backside External Visual Inspection:

This inspection method is for product semiconductor wafers and dice prior to assembly. This test method defines the requirements to execute a standardized external visual inspection and is a non-invasive and nondestructive examination that can be used for qualification, quality monitoring, and lot acceptance.

JESD22-C101

Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components:

This standard describes a uniform method for establishing charged-device model (CDM) electrostatic discharge (ESD) withstands thresholds. The charged-device-model simulates charging /discharging events that occur in production equipment and process.

JESD28

A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress:

This standard describes an accelerated test for measuring the hot-carrier-induced degradation of single n-channel MOSFETs under peak substrate current using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way.

JESD30

Descriptive Designation System for Semiconductor-Device Packages:

Describes a systematic method for generating descriptive designators for packages; emphasis was placed on maintaining and legitimizing existing, commonly used package abbreviations and acronyms.

JESD31

General Requirements for Distributors of Commercial and Military Semiconductor Devices:

This publication identifies the general requirements for Distributors that supply Commercial and Military products.

JESD33

Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line:

This method is intended for determining the temperature coefficient of resistance of thin film metallization, for estimating a mean temperature of a metallization line stressed in an accelerated electromigration stress test, and for using a metallization test line as an ambient-temperature sensor.

JESD35

Procedure for Wafer-Level Testing of Thin Dielectrics:

This standard was developed a s a means for estimating the overall integrity of thin gate oxides and as a tool for driving constant improvement in the thin oxide process.

Annex A (informative) Standards (cont'd)

JESD37

Standard Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method:

This standard enables the user to estimate the parameters of a two-parameter lognormal distribution from complete or singly right-censored independent data samples. Specifically, this standard is intended for analyzing failure-time (tf) data obtained from a stress test of a sample of units when the natural logarithms of the failure -time (ln tf) follow a normal distribution.

JESD38

Standard For Failure Analysis Report Format:

This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

JESD46

Customer Notification of Product/Process Changes by Semiconductor Suppliers:

This standard establishes procedures to notify customers of semiconductor product and process changes. Requirement include: documentation; procedure for classification, notification and customer response; content; and records. Documentation of a suppliers change notification system should set clear and understandable expectation for both the originators of the change and their end customer.

JESD47

Stress-Test-Driven Qualification of Integrated Circuits:

This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

JESD48

Product Discontinuance:

This standard establishes the requirements for timely customer notification of planned product discontinuance, which will assist customers in managing end-of-life supply, or to transition on-going requirements to substitute products.

JESD49

Procurement Standard for Known Good Die (KGD):

This standard provides guidelines and requirements for KGD used in other than conventionally packaged microcircuit or discrete formats. The die described herein are intended to be high quality, reliable bare dice in die form only, for use in a variety of user-defined applications (e.g. multi-chip, modules, hybrid circuits, memory cards, etc.).

Annex A (informative) Standards (cont'd)

JESD50

Special Requirements For Maverick Product Elimination And Outlier Management:
The purpose of the Maverick Product Elimination proposed standard is to identify supplier requirements intended to improve the delivered quality and reliability of electronic assemblies and subassemblies, and to develop the programs and thought processes required to protect the user of electronic components.

JESD60

A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation at Maximum Gate Current Under DC Stress:
This document describes an accelerated test for measuring the hot-carrier-induced change of a single lateral drain p-channel MOSFET under peak gate current using dc bias. Typically, p-channel devices will display maximum parameter changes with the gate biased so as to maximize gate current.

JESD61

Isothermal Electromigration Test Procedure:
This document describes an algorithm for the execution of the Isothermal Accelerated Wafer Level Electromigration Test using computer-controlled instrumentation. There is no limitation to the use of this procedure at lower acceleration levels, down to and including the levels used for the conventional electromigration test.

JESD63

Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature:
This method provides procedures that use linear regression analyses for calculating sample estimates, and their confidence intervals, of the electromigration model parameters for current density and temperature of thin-film metal interconnects used in microelectronic devices.

JESD69

Information Requirements For The Qualification Of Silicon Devices:
This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy.

JESD72

Test Methods And Acceptance Procedures For The Evaluation Of Polymeric Materials:
This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications.

Annex A (informative) Standards (cont'd)

JESD74

Early Life Failure Rate Calculation Procedure For Semiconductor Components:

This standard defines methods for calculating the early life failure rate of a product, using accelerated testing, whose failure rate is constant or decreasing over time. For technologies where there is adequate field failure data, alternative methods may be used to establish the early life failure rate. The purpose of this standard is to define a procedure for performing measurement and calculation of early life failure rates. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and screen strategies to ensure that the ELFR meets customers' requirements.

JESD77

Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices:

The purpose of this standard is to promote the uniform use of symbols, abbreviations, terms, and definitions throughout the semiconductor industry.

JESD78

IC Latch-Up Test:

This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies.

JESD85

Methods For Calculating Failure Rates In Units Of Fits:

This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

JESD86

Electrical Parameters Assessment:

This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device's capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

JESD88

JEDEC Dictionary of Terms for Solid State Technology:

This document is a collection of terms and definitions relating to solid state devices and technology.

Annex A (informative) Standards (cont'd)

JESD89

Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices:

This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a devices SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

JESD89-1

Test Method For Real-Time Soft Error Rate:

This test is used to determine the Soft Error Rate (SER) of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) for errors which require no more than re-reading or re-writing to correct and as used in terrestrial environments. It simulates the operating condition of the device and is used for qualification, characterization, or reliability monitoring. This test is intended for execution in ambient conditions without the artificial introduction of radiation sources.

JESD89-2

Test Method For Alpha Source Accelerated Soft Error Rate:

This test method is offered as standardized procedure to determine the alpha particle Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flipflops) by measuring the error rate while the device is irradiated by a characterized, solid alpha source.

JESD89-3

Test Method For Beam Accelerated Soft Error Rate:

This test is used to determine the terrestrial cosmic ray Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g., flip-flops) by measuring the error rate while the device is irradiated in a neutron or proton beam of known flux. The results of this accelerated test can be used to estimate the terrestrial cosmic ray induced SER for a given terrestrial cosmic ray radiation environment. This test cannot be used to project alpha-particle induced SER.

JESD99

Terms, Definitions, and Symbols for Microelectronics Devices:

This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronic devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed section for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. It lists and defines more than 400 of the most common physical and electrical terms applicable to these devices, and shows the industry-standard symbols and abbreviations that have been established for such terms.

Annex A (informative) Standards (cont'd)

JESD100

Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits:
A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, microcontrollers, memory ICs, and other complex devices.

JESD201

Environmental Acceptance Requirements For Tin Whisker Susceptibility Of Tin And Tin Alloy Surface Finished:
The methodology described in this document is applicable for environmental acceptance testing of tin based surface finishes and mitigation practices for tin whiskers. This methodology may not be sufficient for applications with special requirements, (i.e., military, aerospace, etc.). Additional requirements may be specified in the appropriate requirements (procurement) documentation.

JESD282

Silicon Rectifier Diodes:
This standard provides definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers ratings and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power. (Formerly known as EIA-282-A, ANSI/EIA-282-A-1989.)

JESD284

Test Methods for the Collector - Base Time Constant and for the Resistive Part of the Common Emitter Input Impedance:
This standard defines the test methods that are most generally applicable to alloy-type devices for which simplified equivalent circuits can be used. (Formerly known as EIA-284-A.)

JESD286

Standard for Measuring Forward Switching Characteristics of Semiconductor Diode:
This standard defines measurement methods for forward switching characteristics of semiconductor diodes, to include forward current time characteristics, forward recovery time, peak forward recovery voltage and forward turn on time. (Formerly known as EIA-286-A, ANSI/EIA-286-A-1991.)

JESD306

Measurement of Small-Signal HF, VHF, and UHF Power Gain of Transistors:
This standard defines measurement method for small-signal HF, VHF, and UHF power gain of low power transistors. (Formerly known as RS-306 and/or EIA-306)

JESD307

Voltage Regulator Diode Noise Voltage Measurements:
This standard defines the measurement of noise voltage in a diode voltage regulator in the reverse breakdown region. (Formerly known as RS-307, EIA-307.)

Annex A (informative) Standards (cont'd)

JESD311

Measurement of Transistor Noise Figure at MF, HF and VHF:

This standard defines a test method for the measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. (Formerly known as RS-311 and/or EIA-311-A.)

JESD313

Thermal Resistance Measurements of Conductive Cooled Power Transistor:

This standard defines a test method in measuring thermal resistance for conduction cooled power transistors.

JESD320

Thermal Equilibrium Conditions for Measurement of Diode Static Parameters:

This standard defines a method for achieving thermal equilibrium when measuring temperature sensitive static parameters of signal diodes.

JESD353

The Measurement of Transistor Noise Figure at Frequencies up to 20 KHz by Sinusoidal Signal Generator Method:

This standard defines measuring methods for transistors whose noise has a gauging power distribution, for transistors whose noise has a flat (white) power distribution, and for transistors whose noise has a 1/f (power inversely proportional to frequency) power distribution. (Formerly known as RS-353 and/or EIA-353.)

JESD354

Measurement of Transistor Equivalent Noise Voltage and Equivalent Noise Current at Frequencies of up to 20 KHz:

This standard defines the measurement method for determining values, for device registration purposes, of transistor equivalent noise voltage and equivalent current at frequencies up to 20 KHz. This method is applicable to transistors whose noise has a Gaussian flat (white) or 1/f power distribution. (Formerly known as RS-354 and/or EIA-354)

JESD371

Measurement of Small-Signal VHF-UHF Transistor Short-CircuitForward Current Transfer Ratio:

This standard defines the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit for and current transfer ratio, for preparing data sheets for JEDEC registration of low power transistors. (Formerly known as RS-371 and/or EIA-371.)

JESD372

Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters:

This standard defines the test method to be used for the measurement of admittance parameters for small-signal VHF-UHF transistors. (Formerly known as RS-372 and/or EIA-372.)

Annex A (informative) Standards (cont'd)

JESD381

Method of Diode "Q" Measurements:

This standard defines the method to measure "Q" of the voltage-variable capacitance diode in the low VHF range using an RF admittance bridge. (Approved as ANSI/EIA-381-A-1992, Jul. Became JESD381-A after ANSI expiration.)

JESD398

Measurement of Small Values of Transistor Capacitance:

This standard defines the terminal method for capacitance measurement, with die precautions for shielding of extraneous efforts due to internal leads and metal enclosures. (Formerly known as RS-398 and/or EIA-398.)

JESD471

Symbol and Label for Electrostatic Sensitive Devices:

This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words "ATTENTION- OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES". The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it. (Formerly known as EIA-471.)

JESD625

Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices:

This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that susceptible to damage or degradation from ESD. (Formerly known as EIA-625, that superseded JEP108-B.)

JESD659

Failure Mechanism Driven Reliability Monitoring of Silicon Devices:

This is a standard for the application of statistical reliability monitoring (SRM) technologies to monitor and improve the reliability of silicon devices by continually evaluating product against potential failure mechanisms. (Formerly known as EIA-659 that superseded JESD29)

JESD670

Quality System Assessment:

This proposed standard is for use by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q91 (ISO-999001), ANSI/ASQC Q92 (ISO-9002), and EIA-599. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q94 (ISO-9004) and the Malcolm Baldrige National Quality Award criteria. (Supersedes JESD39)

Annex A (informative) Standards (cont'd)

JESD671

Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems):

This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. (Formerly EIA-671)

JP002

Current Tin Whiskers Theory And Mitigation Practices Guideline:

This document will provide insight into the theory behind tin whisker formation as it is known today and, based on this knowledge, potential mitigation practices that may delay the onset of, or prevent tin whisker formation. The potential effectiveness of various mitigation practices will also be briefly discussed. References behind each of the theories and mitigation practices are provided.

JS-001

Joint Jedec/Esda Standard For Electrostatic Discharge Sensitivity Test - Human Body Model (Hbm) - Component Level

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD). The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels. NOTE Data previously generated with testers meeting all waveform criteria of ANSI/ESD STM5.1-2007 or JESD22A-114F shall be considered valid test data.

JS9702

Monotonic Bend Characterization of Board-Level Interconnects (IPC/JEDEC-9702):

This publication specifies a common method of establishing the fracture resistance of board-level device interconnects to flexural loading during non-cyclic board assembly and test operations.

JS9704

Printed Wiring Board (PWB) Strain Gage Test Guideline (IPC/JEDEC):

This document describes specific guidelines for strain gage testing for Printed Wiring Board (PWB) assemblies. The suggested procedures enables board manufacturers to conduct required strain gage testing independently, and provides a quantitative method for measuring board flexure, and assessing risk levels.

J-STD-001

Requirements for Soldered Electrical and Electronic Assemblies:

This standard describes materials, methods and acceptance criteria for producing soldered electrical and electronic assemblies. The intent of this document is to rely on process control methodology to ensure consistent quality levels during the manufacture of products. It is not the intent of this standard to exclude any procedure for component placement or for applying flux and solder used to make the electrical connection.

Annex A (informative) Standards (cont'd)

J-STD-002

Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires:
This standard prescribes test methods, defect definitions, acceptance criteria and illustrations for assessing the solderability of electronic component leads, terminations, solid wires, stranded wires, lugs and tabs. This standard addresses both visual acceptance and force measurement solderability criteria for both tin-lead as well as lead-free solder processes. This standard also includes a test method for the Resistance to Dissolution/Dewetting of Metallization to verify that metallized terminations will remain intact throughout the assembly soldering processes. This standard is intended for use by both vendors and users. The Amendment 1 now included in this IPC/ECA J-STD-002C adds an appendix that defines a test protocol for wetting balance testing and also allows the use of production solder pastes of appropriate lead-based and lead free compositions for surface mount simulation testing.

J-STD-005

Requirements for Soldering Pastes:
This standard lists requirements for qualification and characterization of solder paste. It references test methods and criteria for metal content, viscosity, slump, solder ball, tack and wetting of solder pastes. Additional support is provided in IPC-HDBK-005, Guide to Solder Paste Assessment (not included with purchase of this standard).

J-STD-020

Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices:
The purpose of this test method is to identify the classification level of plastic IC Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent mechanical damage during the assembly solder reflow attachment and/or repair operation.

J-STD-033

Joint Ipc/Jedec Standard For Handling, Packing, Shipping, And Use Of Moisture/Reflow Sensitive Surface-Mount Devices:
This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033C helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags.

Annex A (informative) Standards (cont'd)

J-STD-075

Classification of Non-IC Electronic Components for Assembly Processes:
J-STD-075 picks up where J-STD-020 left off by providing test methods to classify worst-case thermal process limitations for electronic components. Classification is referenced to common industry wave and reflow solder profiles including lead-free processing. The classifications represent maximum process sensitivity levels and do not establish rework conditions or recommended processes for an assembler. It outlines a process to classify and label non-semiconductor electronic component's Process Sensitivity Level (PSL) and Moisture Sensitivity Level (MSL) consistent with the semiconductor industry's classification levels (J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Devices and J-STD-033, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices).

MIL-DTL-19491

Packaging of Semiconductor Devices:
This specification covers the requirements for the preservation, packing, and container marking of semiconductor devices such as transistors and diodes (FSC 5961).

MIL-HDBK-175

Microelectronic Devices:
This handbook provides information on technology, reliability, testing and design considerations. It is intended as a quick-reference document to provide general guidance for employing the technology.

MIL-HDBK-814

Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices FSC 59GP:
This document addresses the piece-part level system engineering approach to the implementation of an HA program applicable to both neutron and ionizing radiation (ionizing dose) permanent damage derived from nuclear weapon or natural space environments.

MIL-HDBK-1331

Handbook for Parameters to be Controlled for the Specification of Microcircuits:
This handbook describes the parameters required as a minimum for the specification of microcircuits. Parameters, rather than circuits, are considered because circuits vary with the manufacturers involved. Further, circuit designs should be subject to change if improvement results as long as the affected designs are compatible and fully interchangeable

MIL-PRF-19500

General Specification for Semiconductor Devices;
This specification establishes the general performance requirements for semiconductor devices. Four levels of product assurance requirements are provided, differentiated by the prefixes JAN, JANTX, JANTXV, and JANS.

MIL-PRF-38534

General Specification for Hybrid Microcircuits:
This specification establishes the general requirements for hybrid microcircuits and specifies the quality & reliability assurance requirements that shall be met in the acquisition of such devices.

Annex A (informative) Standards (cont'd)

MIL-PRF-38535

General Specification for Integrated Circuits (Microcircuits) Manufacturing:
This specification establishes the general requirements for integrated circuits and the quality and reliability assurance requirements that must be met for their acquisition. Sections outline requirements for Qualified Manufacturer Listing.

MIL-STD-202

Test Method Standard, Electronic and Electrical Component Parts:
This standard establishes uniform methods for testing electronic and electrical component parts, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests.

MIL-STD-750

Test Methods for Semiconductor Devices FSC 5961:
This standard establishes uniform methods for testing semiconductor devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests.

MIL-STD-790

Established Reliability and High Reliability Qualified products List (QPL) System for Electrical, Electronic, and Fiber Optic Part Specification:
This standard is for direct reference in established reliability and high reliability electrical, electronic and fiber optic parts specifications and establishes the criteria for manufacturer's qualified product system.

MIL-STD-883

Test Method Standard, Microcircuits:
This standard establishes uniform methods for testing microelectronic devices suitable for use within Military and Aerospace electronic systems including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations; mechanical and electrical tests; workmanship and training procedures; and such other controls and constraints as have been deemed necessary to ensure a uniform level of quality and reliability suitable to the intended applications of those devices.

NIST Malcolm Baldrige:

The Malcolm Baldrige National Quality Award:
An annual Award to recognize U.S. Companies that excel in quality achievement and quality management. Capitalize on the combined resources of BNQP and collaborating organization to bring value to both organizations and to educate communities about the benefits of using Baldrige for improved organizational performance.

Annex A (informative) Standards (cont'd)

SAE J1879

Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications:

The Robustness Validation approach is a process which requires: (a) specification of requirements based on a Mission Profile, (b) Failure Modes and Effects Analysis (FMEA) to determine relevant failure mechanism associated with these failure mechanisms and assess risk, (c) testing of the device to failure or "end-of-life" for each relevant specification requirement and (d) software controlled functionality. This handbook defines a user methodology to assess the Robustness Margin between the outer limits of the specification and the semiconductor's actual performance during the design and development process, and monitoring mechanisms for insuring reliability throughout the production lifecycle.

TECHAMERICA EIA-554

Method Selection for Assessment of Nonconforming Levels in Part Per Million (PPM):

This standard was developed to provide

1. A uniform method of measurement and calculation of average outgoing quality levels. Minimum sample sizes and a method for aggregating data are provided.
2. A uniform method of assessing quality levels in situations with audit sampling rather than acceptance sampling is performed.

TECHAMERICA EIA-555

Lot Acceptance Procedure for Verifying Compliance with the Specified Quality Levels (SQL) in PPM:

This specification is a means by which PPM nonconformance level requirements can be verified on a lot by lot basis until such time that quality approaches the ultimate objective of near zero nonconformances. It allows a customer to set his quality requirements (Specified Quality Level) and provides a method for verifying that an individual lot meets those quality requirements (SQL). A key feature of this standard is that it provides incentives for suppliers to improve their quality. The lot acceptance portion of this standard requires larger sample sizes when quality declines and smaller sample sizes when quality improves.

TECHAMERICA EIA 557

Statistical Process Control Systems:

This document describes the general requirements of a statistical process control (SPC) system.

Annex A (informative) Standards (cont'd)

TECHAMERICA EIA-584

Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of a Continuous Manufacturing Process:

Conventional attribute sampling plans based upon nonzero acceptance numbers are no longer desirable. In addition, emphasis is now placed on the quality level that is received by the customer. This relates directly to the Lot Tolerance Percent Defective (LTPD) value or the Limiting Quality Protection of MIL-STD-105. Measuring quality levels in percent nonconforming, although not incorrect, has been replaced with quality levels measured in parts per million (PPM). As a result, this standard addresses the need for sampling plans that can argument MIL-STD-105, are based upon zero acceptance number, and address quality (nonconformance) levels in the parts per million range. This document does not address minor nonconformance, which are defined as nonconformances that are not likely to reduce materially the usability of the unit of product for its intended purpose.

TECHAMERICA EIA-585

Zero Acceptance Numerical Sampling Procedure and Tables for Inspection by Attributes of Isolated Lots:

Conventional attribute sampling plans based upon acceptance numbers that permit acceptance of a lot when some allowable number of nonconformances is encountered during inspection are no longer desirable. In addition, emphasis is now placed on the quality level that is received by the customer. This relates directly to the Lot Tolerance Percent Defective (LTPD) value or the Limiting Quality Protection of MIL-STD-105. Measuring quality levels in percent nonconforming, although not incorrect, has been replaced with quality levels measured in parts per million (PPM). As a result, this standard addresses the need for sampling plans that can augment MIL-STD-105, are based upon zero acceptance number, and address quality (nonconformance) levels in the parts per million ranges. This document does not address minor nonconformance, which are defined as nonconformance that are not likely to reduce materially the usability of the unit of product for its intended purpose.

TECHAMERICA EIA681

Assessment Guide for Process Certification:

It is the purpose of this document to provide guidance for companies and registrars to achieve a consistent assessment of a producer's compliance to the requirements to Process Certification (EIA-599). In addition, a technique is provided as an option for the assessment of t producer's level of quality system maturity.

TECHAMERICA EIA-738

Guideline on the Use and Application of Cpk:

This document provides the guidelines for the utilization of Cpk as a process performance monitor. This document defines the process capability index (Cpk), outlines some general methods for estimating Cpk, discusses the advantages, disadvantages, and requirements for some potential applications of Cpk, addresses the use of similar methods of assessing quality improvement, and provides some perspective on the value of Cpk and similar techniques.

Annex A (informative) Standards (cont'd)

TECHAMERICA GEIA-GEB-0002

Reducing the Risk of Tin Whisker-Induced Failures in Electronic Equipment:

This Bulletin provides a brief description of tin whisker formation and describes various methods recommended by government and industry to reduce the risk of tin whisker-induced failures in electronic hardware.

TECHAMERICA GEIA-HB-0005-1

Program Management/Systems Engineering Guidelines For Managing The Transition To Lead-Free Electronics:

This handbook is designed to assist program management and/or systems engineering management in managing the transition to lead-free (Pb-free) electronics to assure product reliability and performance.

Programs may inadvertently introduce Pb-free elements (including piece part finish, printed wiring board finish, or assembly solder) if careful coordination between buyer and supplier is not exercised. For example, piece part manufacturers may not always change part numbers to identify Pb-free finishes, especially if the previous tin-lead (Sn/Pb)-finished piece part has been discontinued. Detailed examination of piece parts and documents at receiving inspection while crucial, may not be sufficient to identify Pb-free piece parts.

TECHAMERICA GEIA-HB-0005-2

Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Lead-free Solder and Finishes:

This document is intended for use as technical guidance by Aerospace system suppliers, e.g., Aerospace system Original Equipment Manufacturers (OEMs) and Aerospace system maintenance facilities, in developing and implementing designs and processes to assure the continued performance, quality, reliability, safety, airworthiness, configuration control, affordability, maintainability, and supportability of high performance aerospace systems (subsequently referred to as AHP) both during and after the transition to Pb-Free electronics.

TECHAMERICA GEIA-HB-0005-3

Rework/Repair Handbook to Address the Implications of Lead-Free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems:

This document provides technical background, procurement guidance, engineering procedures, and guidelines to assist organizations reworking/repairing aerospace and high performance electronic systems, whether they were assembled or previously reworked/repaired using traditional alloys such as SnPb or Pb-free alloys, or a combination of both solders and surface finishes. This document contains a review of known impacts and issues, processes for rework/repair, focused to provide the technical structure to allow the repair technician to execute the task.

TECHAMERICA GEIA-STD-0002-1

Aerospace Qualified Electronic Component (AQEC) Requirements, Volume 1 – Integrated Circuits and Semiconductors:

This Standard defines the minimum requirements for integrated circuits and semiconductors that are to be designated an "Aerospace Qualified Electronic Component (AQEC)". An AQEC Plan will be developed by the manufacturer in order to document compliance with AQEC requirements.

Annex A (informative) Standards (cont'd)

TECHAMERICA GEIA-STD-0005-1

Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead-free Solder:

This standard defines the objectives of, and requirements for, documenting processes that assure customers and regulatory agencies that AHP electronic systems containing Pb-free solder, piece parts, and boards will satisfy the applicable requirements for performance, reliability, airworthiness, safety, and certifiability throughout the specified life of performance.

TECHAMERICA GEIA-STD-0005-2

Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems:

This Standard establishes processes for documenting the mitigating steps taken to reduce the harmful effects of tin finishes in electronic systems.

TECHAMERICA GEIA-STD-0005-3

Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes

This document addresses the evaluation of failure mechanisms, thru performance testing, expected in electronic products containing Pb-free solder. One failure mode, fatigue-failure thru the solder-joint, is considered a primary failure mode in AHP electronics and can be understood in terms of physics of failure and life-projections. Understanding all of the potential failure modes caused by Pb-free solder of AHP electronics is a critical element in defining early field failures/ reliability issues. Grouping of different failure modes may result in incorrect and/or misleading test conclusions. Failure analysis efforts should be conducted to insure that individual failure modes are identified, thus enabling the correct application of reliability assessments and life-projection efforts.

TECHAMERICA GEIA-STD-0006

Requirements for Using Solder Dip to Replace the Finish on Electronic Piece Parts:

This standard defines the requirements for fully replacing pure tin and Pb-free tin alloy finishes with SnPb finishes using robotic and semi-automatic solder dipping. Requirements for qualifying and testing the refinished piece parts are also included.

TECHAMERICA RB9

Failure Mode and Effect Analyses:

This Reliability Bulletin is provided as a guide for engineering and management personnel concerned with Failure Mode and Effect Analyses (FMEA). In addition, it provides information concerning technical and functional relationship of Failure Mode and Effect Analyses to associated disciplines, as for example, Maintainability, Safety, and System Effectiveness Analyses. This Bulletin covers requirements, concepts, interface, procedures and reports of FMEA. This Bulletin should contribute to greater utilization of FMEA results and to the understanding and appreciation of the purpose of FMEA on the part of engineering and management personnel.

Annex A (informative) Standards (cont'd)

TECHAMERICA SSB-1

Guidelines for Using Plastic Encapsulated Microcircuits and Semiconductors in Military, Aerospace and Other Rugged Applications:

This Engineering Bulletin and its annexes provide guidance to Original Equipment Manufacturers (OEMs) in evaluating device manufacturer flows and in selecting cost effective, standard products that meet the performance objective for potential use in many rugged, military, severe, or other environments.

TECHAMERICA SSB-1.001

Qualification and Reliability Monitors:

The scope of this document is to establish the recommended minimum qualification and monitoring testing of plastic encapsulated microcircuits and discrete semiconductors suitable for potential use in many rugged, military, severe, or other environments.

TECHAMERICA SSB-1.002

Environmental Tests and Associated Failure Mechanisms:

This document provides reference information concerning the environmental stresses associated with tests specifically designed to apply to (or have unique implications for) plastic encapsulated microcircuits and semiconductors, and the specific failures induced by these environmental stresses.

TECHAMERICA SSB-1.004

Failure Rate Estimating:

This document provides reference information concerning methods commonly used by the semiconductor industry to estimate failure rates from accelerated test results. These methods are frequently used by OEMs in conjunction with physics of failure reliability analysis to assess the suitability of plastic encapsulated microcircuits and semiconductors for specific end use applications.

UL 94

Tests for Flammability of Plastic Materials for Parts in Devices and Appliances:

These requirements cover tests for flammability of plastic materials used for parts in devices and appliances. They are intended to serve as a preliminary indication of their acceptability with respect to flammability for a particular application.

UL1694

UL Standard for Safety Tests for Flammability of Small Polymeric Component Materials:

These requirements specify a needle-flame test to simulate the effect of small flames which may result from fault conditions within equipment in order to assess the fire hazard by a simulation technique.

This test is applicable to small components which contain materials that cannot be fabricated into standardized specimens in the minimum use thickness and subjected to applicable preselection tests, such as UL 94. Test procedures specified have been determined to be applicable to small components with an overall volume of less than 2500 mm3 (0.15 in3).Test procedures may not be applicable to small components with an overall volume greater than 2500 mm3 (0.15 in3).

Annex B (informative) Rescinded, Cancelled, Withdrawn, or Replaced

These documents are no longer in force and are included for reference only.

ANSI/ISO/ASQ Q9000-3-1997

Quality Management and Quality Assurance Standards:
Part 3: Guidelines for the Application of ANSI/ISO/AQC Q9001-1994 to the Development, Supply, Installation, and Maintenance of Computer Software

ANSI/ISO/ASQ Q9004-2000

Quality Management Systems Guidelines for Performance Improvements
Replaced by ISO 9004:2009 Managing for the sustained success of an organization – A quality management approach.

ANSI/ISO/ASQC Q9003-1994

Model for Quality Assurance in Final Inspection and Test:— E-Standard

ANSI/ISO/ASQ Q9000-2-1997

Quality Management and Quality Assurance Standards Generic Guidelines for the Application of ANSI/ISO/ASQC Q9001-1994, Q9002-1994, and Q9003-1994: Superseded by ANSI/ISO/ASQ Q9000-2005 - Quality management systems: Fundamentals and vocabulary.

ANSI / ESD S3.1

Ionization:
This standard provides test methods and procedures for evaluating and selecting air ionization equipment and systems. It establishes measurement techniques to determine ion balance and charge neutralization time for ionizers. (Withdrawn 1991 Supersceded by ESD STM3.1)

ANSI / ESD S5.1

Human Body Model Electrostatic Discharge Sensitivity Testing:
This standard establishes a procedure for evaluating the ESD sensitivity of components to a defined human body model. It covers test procedures and provides a means of component sensitivity classification. (Withdrawn)

ASQ A8402

Quality Systems Terminology:
Defines the fundamental terms relating to quality assurance, quality control, quality programs, quality systems, and quality concepts as they apply to all areas of the industry. (Withdrawn)

BS CECC 90000

Harmonized System of Quality Assessment for Electronic Components Generic Specification: Monolithic Integrated Circuits:
Visual inspection (testing), Defects, Quality control, Surface defects, Monolithic integrated circuits, Integrated circuits, Circuits, Electronic equipment and components, Quality assurance systems, Assessed quality, Qualification approval, Approval test. (Superseded by BSI BS EN 190000 and BS 9400)

Annex B (informative) Rescinded, Cancelled, Withdrawn, or Replaced (cont'd)

CECC 00114

Rules of PROCEDURE 14. Quality Assessment Procedures:

This standard describes the component approval procedures available under the European CECC system. Issued in the following parts:

P0 - An Introduction to the types of approval available under the CECC System
P1 - Approval of manufacturers and other organizations
P2 - Qualification approval of electronic components
P3 - Capability approval of an electronic components manufacturing activity
P4 – Procedure for Enhanced Assessment of Quality
P5 - Process approval of specialist contractors within the electronic components industry
P6 - Technology approval of Electronic Component Manufacturing
(Withdrawn)

EIA599

National Electronic Process Certification Standard; Government Contractors:

This standard is applicable to suppliers of electronic components, assemblies, equipment and related materials. This standard establishes the requirements to achieve a certified process. The use of this standard is intended for any manufacturing or service company whose goal is to achieve customer satisfaction through continuous improvement. (Replaced by ISO 9000 series.)

FED-STD-209

Environmental Controls (Cleanroom):

This document establishes standard classes of air cleanliness for airborne particulate levels in cleanrooms and clean zones. It prescribes methods for class verification and monitoring of air cleanliness. It also addresses certain other factors, but only as they affect control of airborne particulate contamination. (Cancelled November 2001)

IEC 60695-1-1

Fire Hazard Testing:

This standard provides a) guidance for the preparation of requirements and test specifications for assessing fire hazard of electro-technical products, b) test methods, and c) examples of fire hazard assessment procedures and interpretation of results. (Superseded by IEC 60695-1-10 and IEC 60695-1-11)

JEP88

Thermal Resistance and Thermal Impedance Test Methods for Stud and Base-Mounted Rectifier Diodes and Thyristors:

The test method applies to rectifier diodes of either polarity. The thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat removal from the active semiconductor element. (Rescinded)

JEP96

Guidelines for Nondestructive Pull Testing of Wire Bonds on Hybrid Devices:

This publication establishes basic guidelines for preparing working documents that specify performing nondestructive pull tests of wire bonds on particular hybrid devices. It is not intended that these guidelines evolve into an enforcing document. (Rescinded)

Annex B (informative) Rescinded, Cancelled, Withdrawn, or Replaced (cont'd)

JEP112

Test Method for Qualification and Acceptance of Circuit Support Film for Use in Microelectronic Applications:

This test method covers the minimum requirements that should be in effect for the qualification and acceptance of circuit support films for use in microelectronic applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic device is not compromised. (Rescinded and replaced by JESD72)

JESD62

Outlier Identification and Management System for Electronic Components:

Component quality and reliability can be improved by the implementation of an Outlier Identification and Management system (OUMS) that provides disposition of a typical product with the goal of fine-tuning manufacturing processes and minimizing the probability of user impact. (Rescinded, consolidated into JESD50)

JESD390

Standard Test Procedure for Noise Margin Measurements for Semiconductor Logic Gating Microcircuits:

This standard defines the dc (steady-state) noise margin and the ac (transient) noise margin in semiconductor logic gating microcircuits, and describes the procedures used to measure these parameters. The standardization of the definitions and test procedures is intended to improve the ability to ensure interchangeability of elements by test specification, and to eliminate misunderstandings between manufacturers and users. (Rescinded October 2008)

JIS C 7312

Reliability Assured Complementary MOS Digital Semiconductor Integrated Circuits (Gates):

This Japanese Industrial Standard applies to the complementary MOS digital semiconductor integrated circuits (gate) for which reliability assurance is particularly required, and specifies the reliability assurance requirements form of detail specification, etc. (Withdrawn)

JIS C 7210

General Rules for Reliability Assured Discrete Semiconductor Devices:

This Japanese Industrial Standard specifies such items as a reliability assurance program, qualification test, quality conformance inspection, and a periodic qualification maintenance test common to the discrete semiconductor devices. (Withdrawn)

NCSL Z540-1 (ANSI/ NCSL Z540-1)

Calibration laboratories and measuring and test equipment general requirements:

Standard for calibration and standards laboratories to control calibrations and measurements according to measurement assurance or conventional methods. (Withdrawn July 2007 superseded by ANS/ISO/IEC 17025:2005 for part 1 and ANSI/NCSL Z540.3-2007 for part 2.)

SAE AE-9

Automotive Electronics Reliability Handbook - February 1987

(Cancelled)

Annex B (informative) Rescinded, Cancelled, Withdrawn, or Replaced (cont'd)

TECHAMERICA EIA-591

Assessment of Quality Levels in PPM Using Variables Test Data:

EIA/EIA-591 established the use of variables test data, which simplifies the traditional approach to measure levels of nonconformance using attribute data, whether the results are stated in percent or Parts Per Million (PPM) as the nonconformance levels approach zero. The quantities required to establish a data base for an acceptable confidence level may be in the hundreds of thousands, which makes it virtually impossible for a user to verify these quality levels at an Incoming Inspection facility. (Withdrawn)

TECHAMERICA RB4-A

Reliability Quantification:

(Withdrawn, no replacement)

Annex C (informative) Differences between JEP70C and JEP70B

This Annex briefly describes most of the changes made to entries that appear in this publication, JEP70C, compared to its predecessor, JEP70B (October 1999).

Clause	Description of change
3	Changed organization to a tables based format.
3	Added documents
Annex B	Added “Rescinded” section and moved outdated documents there.

Standard Improvement Form **JEDEC** JEP70C

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


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